Hall Ticket Number:

Code No. : 15345 S N

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.E.E.) V-Semester Supplementary Examinations, June-2023

Digital Electronics

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	What are the most common types of logic gates, and what are their basic operations?	2	1	1	1,2
2.	Convert the following : i) $(3B8)_{16} = (?)_{10}$ ii) $(4528)_{10} = (?)_{16}$	2	3	1	1,2
3.	Draw three variable K-map format.	2	2	2	1,2
4.	What is a multiplexer and how it is used to select one of the several input signals?	2	1	2	1,2
5.	Write the excitation table of D flip flop.	2	2	2	1,2
6.	Define modulus of a counter? Write down the number of flip flops required for mod-5 counter?	2	2	2	1,2
7.	What is the settling time of a DAC and how does it impact its performance?	2	1	3	1,2
8.	How signal-to-noise ratio of an ADC is used to evaluate its operation?	2	4	3	1,2
9.	What is a Read only memory (ROM), how it is used to store data or instructions?	2	1	4	1,2
10.	Discuss programmable logic devices?	2	2	4	1,2
	Part-B (5×8 = 40 Marks)				
11. a)	Discuss the following number systems with examples: Decimal, Binary, Octal, and Hexadecimal	4	2	1	1,2
b)	Compare the parameters of TTL, ECL and CMOS logic families.	4	2	1	1,2
12. a)	Minimize the following expression using K-map. $f(P, Q, R, S) = \Sigma m (0, 1, 4, 5, 7, 8, 9, 12, 13, 15)$.	4	3	2	1,2
b)	Describe function of full adder circuit with its truth table, K-map simplification and logic diagram.	4	3	2	1,2
13. a)	Describe the working of SR Flip-Flop with Truth Table and Logic diagram.	4	3	2	1,2
b)	Design 3-bit synchronous counter and draw output waveform.	4	3	2	1,2

Contd... 2

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14. a)	Describe the working principle of Successive approximation type ADC with the help of block diagram.	4	3	3	1,2
b)	What are the differences between a binary weighted DAC and a R-2R ladder DAC?	4	1	3	1,2
15. a)	Compare the following (i) Volatile with Non-Volatile memory. (ii) SRAM with DRAM memory.	4	2	4	1,2
b)	Draw and explain block diagram of Programmable array logic.	4	2	4	1,2
16. a)	Draw the symbol and write logic expression and truth table of the two input universal logic gates.	4	2	1	1,2
b)	Design a two bit magnitude comparator using logic gates.	4	4	2	1,2
17.	Answer any ***two*** of the following:				
a)	Describe the operation of 4 bit PISO shift register with the help of block diagram.	4	2	2	1,2
b)	Explain the working principle of R-2R ladder type DAC with the help of neat diagram	4	1	3	1,2
c)	Implement the following function using PLA. $F1(A,B,C)= \sum(0,1,,2,4)$ $F2(A,B,C)=\sum(0,5,6,7)$	4	4	4	1,2

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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